Remarks

In a sixth Office Action made Final dated March 3, 2008, claim 21 was rejected under 35 U.S.C. § 103 over U.S. Patent No. 5,926,710 to Tseng in view of U.S. Patent No. 6,010,931 to Sun et al. (hereafter, "Sun"). In addition, claims 1, 2, 5, 10, 12, and 14 were rejected under 35 U.S.C. § 103 over Tseng in view of Sun and U.S. Patent No. 6,806,549 to Tomita; claim 3 was rejected under 35 U.S.C. § 103 over Tseng in view of Sun, Tomita, and U.S. Patent Pub. No. 2002/0168830 to DeBoer et al.; claim 8 was rejected under 35 U.S.C. § 103 over Tseng in view of Sun, Tomita, and U.S. Patent No. 6,010,955 to Hashimoto; and claim 9 was rejected under 35 U.S.C. § 103 over Tseng in view of Sun, Tomita, Hashimoto, and U.S. Patent No. 6,479,341 to Lu. Additionally, claim 13 was rejected under 35 U.S.C. § 103 over Tseng in view of Sun, Tomita, and U.S. Patent No. 5,817,562 to Chang et al.; claim 15 was rejected under 35 U.S.C. § 103 over Tseng in view of Sun, Tomita, and U.S. Patent No. 5,779,927 to Lo; claims 16-19 were rejected under 35 U.S.C. § 103 over Tseng in view of Sun, Tomita, and U.S. Patent Pub. No. 2002/0064968 to Kim et al.; and claim 20 was rejected under 35 U.S.C. § 103 over Tseng in view of Sun, Tomita, and U.S. Patent No. 6,342,416 to Kim et al.

Claims 1-3, 5, 8-10, and 12-21 are pending for consideration.

Referring to remarks made by applicants in the previous response filed December 5, 2007 (hereafter "Previous Response"), the Office Action states:

> In response to the argument, examiner states that the argument is not persuasive because portions of source/drain regions (80 and 84) are exposed after etching even though the source/drain region 82 is covered with the insulating layer 96 and also the spacer 64 is exposed after the etching process (figure 8).

However, applicants again submit that Sun, as relied upon, fails to disclose "performing the dry etching process to etch the first interlayer insulating film until portions of the etch stop layer disposed over the source region, the drain region and the first and second sidewall spacers are exposed," as recited in claim 21.

Applicants submit that source/drain regions 80 and 84 of Sun cannot be characterized as the source region and the drain region recited in claim 21. Claim 21 recites "forming **a gate** on a device formation region of a semiconductor substrate, and

forming source and drain regions in the device formation region of the semiconductor substrate **adjacent respective sides of the gate**." Thus, applicants submit that the source region and the drain region recited in claim 21 are formed adjacent respective sides of **a single gate** (i.e., the same gate). However, source/drain regions 80 and 84 are not formed adjacent respective sides of a single gate. Rather, FIG. 8 of Sun shows that source/drain regions 80 and 84 are adjacent to different gate electrodes 56. Thus, applicants submit that source/drain regions 80, 84 cannot be characterized as the source region and the drain region recited in claim 21.

Therefore, for at least the reason set forth above and the reasons set forth in the Previous Response, applicants submit that the combination of Tseng and Sun proposed in the Office Action fails to disclose "performing the dry etching process to etch the first interlayer insulating film **until portions of the etch stop layer disposed over the source region, the drain region** and the first and second sidewall spacers are exposed," as recited in claim 21.

The Office Action also states that "[a]s to the etching of buffer layer with wet etching, examiner pointed out that Sun illustrates that the etching stop layer along with the dielectric layer can be etched using plasma or alternatively, wet etching can be performed to remove the etch stop layer and cleaned (col.9, 5-13)." However, regardless of whether Sun discloses wet etching, applicants again submit that Sun, as relied upon, fails to disclose "wet etching the buffer layer and the etch stop layer **to expose the source region, the drain region** and the first and second sidewall spacers," as recited in claim 21, wherein the source region and the drain region are formed adjacent respective sides of a gate, as in claim 21. The Office Action states that

> Sun further teaches after the etching steps not only the surfaces of the source, drain regions 80, 84 but also the spacer 64 are exposed (column 9, lines 5-8) which thereby reads on, wet etching the buffer layer and the etch stop layer to expose the source region, the drain region and the sidewall spacers.

However, as noted above, source/drain regions 80 and 84 of Sun cannot be characterized as the source region and the drain region recited in claim 21 because the source region and the drain region recited in claim 21 are formed adjacent respective sides of **a single gate** (i.e., the same gate), while source/drain regions 80 and 84 of Sun are not. Thus, applicants submit that the combination of Tseng and Sun proposed

in the Office Action fails to disclose "wet etching the buffer layer and the etch stop layer **to expose the source region, [and] the drain region**," as recited in claim 21, for at least that reason.

Therefore, applicants request that the stated rejection of claim 21 be withdrawn for at least the reasons set forth above and the reasons set forth in the Previous Response.

In addition, similar to claim 21, claim 1 recites

> forming a gate on a device formation region of a semiconductor substrate, and forming source and drain regions in the device formation region of the semiconductor substrate adjacent respective sides of the gate . . .
> dry etching the first interlayer insulating film until portions of the etch stop layer disposed over the source region, the drain region and the sidewall spacers are exposed . . .
> wet etching the etch stop layer to remove the portions of the etch stop layer disposed over the source region, the drain region and the sidewall spacers.

Applicants submit that Tomita, as relied upon in the Office Action, fails to cure all of the above-noted deficiencies of the proposed combination of Tseng and Sun. Thus, applicants request that the stated rejections of claim 1 and its dependencies (which are claims 2-3, 5, 8-10, and 12-20) be withdrawn at least for reasons similar to those set forth above and those set forth in the Previous Response regarding claim 21.

Additionally, applicants submit that source/drain regions 80 and 84 of Sun cannot be characterized as the source region and the drain region recited in both claim 1 and claim 21 for the additional reason that each of source/drain regions 80 and 84 would be conventionally understood to be a source region on which a storage electrode is formed, while source/drain region 82 would be conventionally understood to be a common drain to which a bit line is connected. Applicants submit that FIG. 11 of Sun illustrates a charge storage capacitor formed on each of source/drain regions 80 and 84, and a bit line contact 112 connected to source/drain region 82. (See Sun at column 9, line 14, to column 10, line 34).

Applicants respectfully request reconsideration of the stated rejections and withdrawal of the stated rejections.

Respectfully submitted,

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